WHAT IS CLAIMED IS:

1. A BIST (built-in self test) circuit comprising:

a controller for controlling a self-testing operation of a memory chip embedded in an integrated circuit;

an address generator for generating pseudo-random address patterns under control of the controller;

a data generator for producing test data associated with data backgrounds of the address bits under the control of the controller; and

a comparator for comparing the test data with memory data output from the memory chip to detect, a defect, if any, of the memory chip.

2. The circuit of claim 1, wherein the controller operates using an algorithm that counts the data backgrounds of the address bits in a single-order.

3. The circuit of claim 1, wherein the address generator comprises:

a plurality of linear feedback shift registers (LFSRs) serially connected to each other for producing the pseudo-random address patterns, the pseudo-random address patterns being single-order pseudo-random address patterns; and

a register controller for controlling the plurality of LFSRs. .

4. The circuit of claim 3, wherein the a plurality of LFSRs comprise a counter for counting the address bits to produce the pseudo-random address patterns.

5. The circuit of claim 1, wherein the data generator comprises:

a first multiplexer for receiving the address bits and a ground voltage as input values and selecting one of the input values in response to a first control signal from the BIST controller; and

a second multiplexer for producing the test data from the output of the first multiplexer, in response to a second control signal from the controller.

6. The circuit of claim 5, wherein the first control signal comprises a current data background of the address bits, and the second control signal comprises a complemented data background of the address bits.

7. The circuit of claim 1, wherein the address generator comprises:

a first linear feedback shift register for producing a first group of the pseudo-random address patterns by counting the address bits;

a second linear feedback shift register, serially connected to the first linear feedback shift register, for producing a second group of the pseudo-random address patterns by counting the address bits; and

a register controller for controlling the first and second linear feedback shift registers such that the first linear feedback shift register counts lower bits of the address bits and the second linear feedback shift register counts upper bits of the address bits or the first linear feedback shift register counts upper bits of the address bits and the second linear feedback shift register counts lower bits of the address bits.

8. The circuit of claim 7, wherein the pseudo-random random pattern comprises a single-random pseudo-random address pattern.

9. The circuit of claim 7, wherein the second linear feedback shift register produces the second group of the pseudo random address patterns whenever the first linear feedback shift register produces all the first group of the pseudo random address patterns.

10. The circuit of claim 1, wherein the data background of the address bits comprises data combinations that two random memory cells having mutually different addresses have.

11. A method for performing self-testing operation on a memory chip embedded in an integrated circuit, comprising the steps of:

counting address bits to produce test addresses of pseudo-random address patterns;

producing test data according to the test address and data backgrounds of the address bits; and

comparing the test data with memory data output from the memory chip to determine whether a defect exists.

12. The method of claim 11, wherein the step of counting the address bits comprises the step of counting the data backgrounds of the address bits in a single-order.

13. The method of claim 12, wherein the step of counting the address bits further comprises the steps of:

counting lower bits of the address bits to produce a first group of the pseudo-random address patterns; and

counting upper bits of the address bits to produce a second group of the pseudo-random address patterns.

14. The method of claim 11, wherein the step of producing the test data comprises the steps of:

receiving the address bits and a ground voltage as input values;

selecting one of the input values in response to a first signal, the first signal comprising information about a current data background of the address bits; and

producing the test data in response to the selected input value and a second signal, the second signal comprising information about a complemented data background of the address bits.